09/769,976

L Number	Hits	Search Text	DB	Time stamp
1	11	power$4-down with (memory adj cartridge$)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:15
2	1	("6640282").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:01
3	1		USPAT	2003/11/03 15:04
4	1		USPAT	2003/11/03 15:04
5	1		USPAT	2003/11/03 15:11
6	10	power$4-down with remov$4 with cartridge$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:33
7	12	power$4-up with remov$4 with cartridge$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:24
8	4	(power$4-up with remov$4 with cartridge$) not (power$4-down with (memory adj cartridge$))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:28
9	3627	(714/?).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:28
10	3049	(710/?).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:28
11	0	(710/102).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:29
12	0	(710/103).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:31

13	388	(710/301).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:10
14	286	(710/302).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:31
15	612	(710/104).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:31
16	2283	(711/?).ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:31
17	56918	(remov$4 or insert$4) with cartridge$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:33
18	2148	(power$4-down) and power$4-up	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:33
19	897774	(remov$4 and insert$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:33
20	649	((power$4-down) and power$4-up) and ((remov$4 and insert$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:34
21	1207	((710/301).ccls.) or ((710/302).ccls.) or ((710/104).ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:34
22	19	(((power$4-down) and power$4-up) and ((remov$4 and insert$4))) and (((710/301).ccls.) or ((710/302).ccls.) or ((710/104).ccls.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:37

23	1572	memory adj cartridge$	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:38
24	2	((((power$4-down) and power$4-up) and ((remov$4 and insert$4))) and (((710/301).ccls.) or ((710/302).ccls.) or ((710/104).ccls.))) and (memory adj cartridge$)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:39
25	8753	((714/?).ccls.) or ((710/?).ccls.) or ((711/?).ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:39
26	7	(((714/?).ccls.) or ((710/?).ccls.) or ((711/?).ccls.)) and ((power$4-down) and power$4-up) and ((remov$4 and insert$4)) and (memory adj cartridge$)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:43
27	185	alter$4 with (memory adj capacity)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:06
28	36724	configur$4 with memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:49
29	16	(alter$4 with (memory adj capacity)) and (configur$4 with memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 15:50
30	9	((remov$4 or insert$4) with cartridge$) and ((power$4-down) and power$4-up) and (((714/?).ccls.) or ((710/?).ccls.) or ((711/?).ccls.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:02
31	1	resynchroniz$4 with cartridge$ with lockstep	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:05
32	797	((power$4-down) and power$4-up) and insert$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:06

33	7649	increas$4 with (memory adj capacity)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:06
34	15	(((power$4-down) and power$4-up) and insert$4) and (increas$4 with (memory adj capacity))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:06
36	3	(((remov$4 or insert$4) with cartridge$) and ((power$4-down) and power$4-up)) and (((710/301).ccls.) or ((710/302).ccls.) or ((710/104).ccls.))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:11
37	11	(((remov$4 or insert$4) with cartridge$) and ((power$4-down) and power$4-up)) and (increas$4 with (memory adj capacity))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:12
38	9	(((remov$4 or insert$4) with cartridge$) and ((power$4-down) and power$4-up)) and non-redundan$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:13
39	2	("6098132").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:15
40	1		USPAT	2003/11/03 16:13
41	1		USPAT	2003/11/03 16:14
35	81	((remov$4 or insert$4) with cartridge$) and ((power$4-down) and power$4-up)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:18
42	84	"5822547"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:19
43	20	(("5822547") or ("5781744") or ("5768541") or ("5734841") or ("5671368") or ("5636347") or ("5629836") or ("5625238") or ("5581712") or ("5555510")).PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:23
44	8	(("5386567") or ("5310998") or ("5247619") or ("4835737")).PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/03 16:23

US-PAT-NO: 4103326

DOCUMENT-IDENTIFIER: US 4103326 A

TITLE: Time-slicing method and apparatus for disk drive

---------- KWIC ---------

Detailed Description Text - DETX (3):
A disk drive 10 incorporating the control system of the present invention therein is shown in FIGS. 1-6. The disk drive 10 includes a main support frame or casting 20 (FIGS. 2 & 3) about which a housing cover 22 (FIG. 1) is mounted by suitable mounting means (not shown). The housing cover 22 includes a front portion 24 in which a control and display panel 26 is mounted. A presently preferred control and display panel 26 and the switches and lights included thereon will be described in more detail below. The front portion 24 is hinged by suitable means (not shown) about its inward most lower edge so that it may be swung open. In this manner, a disk **cartridge** 28 including a disk 16a therein may be **inserted** into the disk drive 10 and loaded about a drive spindle 30 for rotating the disk 16a about the axis of the spindle 30. The disk drive 10 may alternatively be of the top loading variety.

Detailed Description Text - DETX (5):
The lower portion 42 of the spindle 30 is preferably in the form of a cylindrical shaft having a lower hub 42 fixedly connected about its periphery by suitable connecting means (not shown). The hub 48 extends sufficiently in a radial direction so that that inner-most portion of the lower surface of a disk 16d is supported thereby (see FIG. 3). The disk 16d constitutes the lowest disk in a stacked array of three coaxially aligned disks 16b - 16d which are permanently mounted in the disk drive 10. This is to be distinguished from the disk 16a which is included in the **cartridge** 28 which is **removable** from the disk drive. The specific manner in which the **cartridge** 28 may be **inserted and removed** from the disk drive 10 does not form part of the present

invention and
so will not be described in detail herein. It should be noted, however, that
any suitable well known cartridge loading apparatus may be employed. It should
be further noted that any one or more of the disks 16a - 16d may be deleted
from the drive 10, if desired. In fact, one model of the drive may not contain
any fixed disks therein, if such is desired.

Detailed Description Text - DETX (40):
In describing the control system employed in the disk drive 10, it would
first be helpful to review the nature of the switches and indicator lights
included on the control and display panel 26 shown in FIG. 1. A START/STOP
switch 306 is included in order to provide a means for the operator to start
and stop the disk drive 10. The **removable cartridge** 28 (FIGS. 2 and 3) may be
inserted or removed when the switch 306 is in the STOP position and a
TRANSITION indicator light 308, to be described below, is extinguished.

Switching to the START position will cause the control system to bring the disk
drive up to normal operation speed in about 30 seconds. When the switch is
again moved to the STOP position, the disk drive decelerates to a stop in about
30 seconds, after which the TRANSITION light goes out and the cartridge 28 may
be interchanged.

Detailed Description Text - DETX (42):
The display panel 26 also includes a pair of READY indicator lights 310 and
312. READY light 310 is associated with the upper unit -0 and READY light 312
is associated with the lower unit -1. When the READY lights are lit, this
indicates to the operator that the drive spindle 30 is up to proper speed, that
the heads 14a - 14h are in position over track zero (0) on their respective
disk surfaces, and that no other conditions exist that would prevent a track
seek, read or write operation from being carried out. The lights 310 and 312
will be extinguished when the START/STOP switch 306 is set to the STOP
position. If the drive 10 is operated without the **removable cartridge** 28 in
place, only the READY indicator light 132 can come on.

Detailed Description Text - DETX (147):
The sequence status port 536 has six active inputs (bits .phi.-5). A first input (bit .phi.) is adapted to receive a **CARTRIDGE** OUT signal which will be true when no **cartridge** 28 has been **inserted** into unit .phi. of the drive 10. A suitable sensor (not shown) capable of detecting the non-presence of a cartridge 28 is provided in the drive. This sensor generates the CARTRIDGE OUT signal whenever, following start of the drive 10, a cartridge 28 is not loaded therein.

Detailed Description Text - DETX (243):
Reference is now had to FIGS. 26-31 which depict the **power-up** routine. The first two operations are hardware implemented. Thus, the voltage level detector 518 (FIG. 11) determines if the correct d-c voltage levels are present. If no, it keeps looking until they are. When they are, the clock 516 applies a RESET command on line 519 to reset the microprocessor 500. The following operations are software implemented and are carried out as well during a status sequence (STSEQ) routine. In accordance with the routine, the microprocessor 500 is disabled from responding to the INTERRUPT signals on line 517. Then, all input and output ports and latches are cleared. This operation is followed by clearing the RAMS 502 and then initializing a "stack pointer" located in the microprocessor 500. The stack pointer is a register containing an address identifying a particular memory location in a push-down stack in the microprocessor 500.

Detailed Description Text - DETX (252):
When the sector computation for unit 1 is completed, the processor looks to see whether the sector count for unit .phi.as stored in a register in RAM, is equal to zero. If yes, then the processor executes a HLR 1 routine to be described below.. If no, the processor looks to see whether the sector count for unit .phi.equals the sector count for unit 1, stored in another RAM location. Such inquiry is effected by the microprocessor 500 fetching and comparing the sector counts for units .phi.and 1 from RAM. If the sector counts for units .phi.and 1 are not equal, a mismatch has occurred. The

processor determines then whether such mismatch has occurred twice. If not,
the SCCMPR routine is begun again. If it has occurred twice, or either a
one-second time period inquiry resulted in a positive determination, then the
processor sets bit (5) in the STATUS B byte register in RAM, i.e. ILLEGALLY
SECTORED CARTRIDGE, and begins executing a **power-down** (PWRDWN) routine to be
described below.

Current US Cross Reference Classification - CCXR (1):
710/1

US-PAT-NO: 4103326

DOCUMENT-IDENTIFIER: US 4103326 A

TITLE: Time-slicing method and apparatus for disk drive

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described below.

Current US Cross Reference Classification - CCXR (1):
710/1

US-PAT-NO: 6122131

DOCUMENT-IDENTIFIER: US 6122131 A

TITLE: Adaptively-controlled disk drive assembly

---------- KWIC ---------

Brief Summary Text - BSTX (7):
Several problems inherent of a disk drive assembly become increasingly problematical, however, when attempts are made to provide a disk drive assembly of such improved performance, **increased memory capacity,** smaller size, and lower cost.

Brief Summary Text - BSTX (12):
Therefore, when designing and manufacturing disk drive assemblies with the goal of providing a disk drive assembly of improved performance and **increased memory capacity,** consideration must be given to the aforementioned problems.

Brief Summary Text - BSTX (13):
What is needed is a disk drive assembly of improved performance, **increased memory capacity,** and reduced cost which reduces the aforementioned problems associated with disk drive assemblies.

Brief Summary Text - BSTX (17):
The present invention advantageously provides a disk drive assembly, and an associated method therefor, of improved performance characteristics and **increased memory capacity,** provided at an economical cost.

Detailed Description Text - DETX (28):
five-step, 12 dB range input attenuator to extend AGC (automatic gain control) range, an ENDEC which supports 16/17 and 8/9 codes, a programmer 1, 2, 4, or 8-bit wide controller data interface, and adaptive amplitude asymmetry cancellation, useful with an MR head transducer. The read channel circuit 210 is permitted to be powered by a single +5 V supply exhibiting 1050 mW full-power nominal at a highest data rate, and less than 15 mW during **power-down** modes. Three programmable, 5-bit current DACs provide

independent
R/W head bias control, T/A threshold. Communications to the read channel
circuit 210 can be provided by way of a 40-MHz serial interface, and a servo
Adc provides 9-bit analog-to-digital conversion of servo burst amplitudes.

Detailed Description Text - DETX (41):
In a poorly-mounted drive, overall write seek performance is slowed down to
achieve approximately one offtrack condition in 256 write seeks provided that
the mounting is not so bad that the maximum settle count cannot prevent a
determination that the actuator has settled before the disk drive assembly has
stopped moving. Conversely, in a well-mounted drive, write seeks are performed
very quickly. The maximum number of seeks without the occurrence of an offtrack condition required to decrement the settlement count is high enough to
be sure that the disk drive assembly is mounted in a stable environment, but
not so high that an unreasonably long number of seeks are required to be
successfully performed prior to decrementing the count. When **powering-up,** the
minimum number of settle counts are first utilized. If the **power-up** occurs in
an environment susceptible to overshoot, a single occurrence of an offtrack
condition increases the settle count by one so that the maximum settle count is
quickly reached. In one exemplary embodiment, the minimum settle count for
non-sequential write seeks is four and the maximum settle count is ten.

Detailed Description Text - DETX (56):
Manufacturing variances of mechanical airlocks sometimes do not ensure that
the airlock opens at a speed beneath that of the operating speed of the disk
drive assembly and to close at a rotational speed great enough to ensure that
an electronic return spring, whose energy is generated by the spinning down of
a motor on power off of the drive can keep the MR head transducers parked in
the disk landing zone until after the airlock is closed. To better ensure that
the mechanical airlock is operable as intended, in an embodiment of the present
invention, the spindle motor, upon **power-up,** is caused to rotate at a rotation
speed higher than a nominal rotational speed. Once the higher speed is

reached, the spindle motor coasts down to the nominal rotational speed.

Detailed Description Text - DETX (57):
A time out procedure is used in the event that a spindle motor is incapable of achieving the increased rotational speed. For instance, the spindle motor is instructed to spin up to the increased rotational speed, e.g., 5800 rpm, until such a rotational speed is achieved or a selected time period, e.g., thirteen seconds, times out. And, a maximum, overall time out at which to achieve the increased rotational speed is a second, selected rotational speed, such as eighteen seconds. The two time outs should not overlap. Selection of the time of the first time out should be long enough subsequent to motor **power-up** so that the worst-case motor under worst-case conditions (i.e., high temperature and low voltage) shall be able to achieve a rotational speed of, here, 5400 rpm. Otherwise, the disk drive assembly might utilize two time outs to attempt an overspin, or in the case of overlapping time outs, the disk drive assembly shall fail to reach the desired rotational speed if unable to reach the overspeed

Detailed Description Text - DETX (59):
FIG. 11 illustrates a method, shown generally at 382, of operation of an embodiment of the present invention by which to effectuate the increased **power-up** rotational speed of the spindle motor. First, and as indicated by the block 384, the nominal spindle rotational speed is set. Then, and as indicated by the decision block 386, a determination is made as to whether the disk drive assembly is to be **powered-up**. If not, the no branch is taken back to the block. Otherwise, the yes branch is taken to the block 388, and the spindle motor is rotated at a nominal rotational speed in excess of the nominal rotational speed.

Detailed Description Text - DETX (64):
FIG. 12 illustrates the method, shown generally at 422 of an embodiment of the present invention by which to facilitate opening of the airlock of a disk drive assembly. First, and as indicated by the decision block 424, a

determination is made as to whether the disk drive assembly is to be **powered-up**. If not, the no branch is taken back to the decision block.

Otherwise, the yes branch is taken to the block 426 and the spindle motor is actuated to rotate at a first rotational speed in excess of a nominal rotational speed. An attempt is made, as indicated by the block 428, to read the servo address marks stored on the data disk of the disk drive assembly. A determination is made, as indicated by the decision block 432, as to whether the servo address marks have been detected. If so, the airlock is opened, and the yes branch is taken to the end block 434.

Detailed Description Text - DETX (82):
Selected tracks in the read zone of a data disk are allocated to be used for **power-up** calibration. Indications of the exact location of such calibration tracks are hard-coded in a read only memory. If, however, the calibration track is a bad track, the disk drive assembly fails. Some disk drive assembly instructions, however, permit a small number of bad data tracks in a data zone without precipitating failure of the disk drive assembly. Therefore, it might be desirable not to cause a disk drive assembly to fail if a bad track happens to be a calibration track. By offsetting the location hard-coded in a read only memory with an offset value, a track, other than a bad calibration track, can instead be accessed. Thereby, the disk drive assembly is operable without requiring the calibration tracks to be good.

Detailed Description Text - DETX (83):
FIG. 16 illustrates a method, shown generally at 542 of an embodiment of the present invention by which to offset track location values hard-coded in a read only memory. Once offset, a track other than the calibration track is accessed during **power-up**.

Detailed Description Text - DETX (84):
First, and as indicated by the block 544, the location of the track to be accessed during **power-up** calibration is retrieved from a read only memory. Then, and as indicated by the block 556, an attempt is made to access the

calibration track identified in the read only memory. Thereafter, a determination is made, as indicated by the decision block 558, as to whether the track can be accessed. If so, the yes branch is taken to the end block 562. Otherwise, if the track is bad, the track cannot be accessed, and the no branch is taken to the block 564. The track number of the track to be accessed is altered by a selected offset number, e.g., the number of retries by which an attempt to read a track is made. Then, as indicated by the block 566, the new track is attempted to be accessed.

Detailed Description Text - DETX (86):

Tolerances of MR head transducers require that different bias currents be applied to different MR head transducers to form signals of similar values. Therefore, bias currents applied to MR head transducers must be selectable. And, while the gain of a preamplifier circuit of the disk drive assembly can be controlled by a closed-loop, AGC (automatic gain control) circuit, such a circuit typically should not be used when flying the MR head transducer over DC-erased areas if a disk, such as might occur during **power-up** of the disk drive assembly. During such periods, a pre-selected, fixed gain value may be used. However, because of the variability of MR head transducer construction, a single default value might not provide an acceptable gain value for all disk drive assemblies. As the values of the head transducer gain and the values of the preamplifier gain cannot be predetermined, a manner by which to adaptively select such values permits better assurances that the disk drive assembly shall be properly functional. During operation of an embodiment of the present invention, tables are created in which various values of MR head transducer bias and AGC values are stored. In a subroutine which is called each time in which a lock is to be made to SAMs, all of the possible combinations of values are iterated, and selection is made of the best combinations of values to utilize at a particular disk drive assembly. The actuator bias current may further be increased or decreased depending upon the direction of movement of the MR head transducer, either toward the data disk outer diameter or

the inner
diameter.

Detailed Description Text - DETX (90):
In an embodiment of the present invention, an internal thermistor provides
an indication of excessive levels of thermal energy generation. If excess
levels of thermal energy are detected, a programmable delay time is **inserted**
after the seeks so that there is a delay before reporting completion of the
seek. The same delay mechanism can be used to permit a delay to be **inserted**
after all long seeks in the event that performance

Claims Text - CLTX (19):
13. The disk drive assembly of claim 1 further comprising a rotational
position sensor for sensing rotational positions of said spindle of said
spindle motor, wherein said controller utilizes sensed rotational positions
sensed by said rotational position sensor to commute stator windings of said
spindle motor during initial **power-up** of said spindle motor.

US-PAT-NO: 5590374

DOCUMENT-IDENTIFIER: US 5590374 A
See image for Certificate of Correction

TITLE: Method and apparatus for employing a dummy read command to automatically assign a unique memory address to an interface card

---------- KWIC ---------

Brief Summary Text - BSTX (5):
The personal computer comprises a housing containing a module card rack for holding and interconnecting electronic modules. When the housing is opened, electronic modules are **inserted** into the rack and connected to a mother board which is located at an end of the computer housing opposite the opening of the housing. The mother board provides the electrical interconnections between modules in the computer including the AT bus, power, and grounds. A user can alter the capability of the personal computer by adding or removing computer modules from the computer housing. For example, **memory capacity** may be **increased by inserting** a RAM (Random Access Memory) module into the housing.

Brief Summary Text - BSTX (7):
In existing systems, one type of add-on card is an Ethernet interface module for interfacing between the AT bus and an Ethernet network system. The requirements of the Ethernet are described in detail in Information Processing Systems--Local Area Networks--Part 3: Carrier sense multiple access with collision detection (CSMA/DC) access method and physical layer specifications, International Standard ISO, 8902-3: 1989, ANSI/IEEE Std 802.3--1988, published by Institute of Electrical and Electronics Engineers, Inc., 1989, the subject matter of which is incorporated herein by reference. Also, in existing systems, when a memory address conflict is detected, it is necessary to **power-down** the system and remove from the system the add-on card that is suspected of having a conflict, alter its configuration by whatever means that are provided on the module, and then replace it in the system and power

up and
retest the modules's operation. (The means used in existing systems for
altering base addresses are moveable jumpers or switches.) The CPU again
executes its initialization routine, and, if another memory base address
conflict is detected, the process of removing the module and physically
changing its memory base address is repeated, until the memory conflict is
eliminated. If no memory conflict is detected, the CPU continues executing its
initialization routine.

Brief Summary Text - BSTX (10):
Existing systems with EEPROM based configuration resolve conflicts in the
I/O base address by a method paralleling the method for resolving an address
conflict on jumper or switch based designs. In particular, for the Ethernet
module with an EEPROM based configuration the user of the computer first powers
on the computer. During the CPU initialization routine, when an I/O memory
address conflict is detected, the user must remove the module from the first
computer and **insert** it into a second system having no I/O base address
conflicts. The user may then alter the I/O address of the module by rewriting
the EEPROM. After which, the module now having its original configuration
changed may be reinstalled in the original system.

Brief Summary Text - BSTX (11):
The method for resolving address conflicts is labor intensive, expensive,
and subject to operator error. The process requires removing a module from the
first computer, **inserting** it into the second computer, powering it up and
reconfiguring it in the second system, removing it from the second system,
wires on the module, reinserting it into and retesting it in the first system,
and repeating this process until all conflicts are eliminated. These steps
each require labor for performing them and are thus time consuming. The added
time for set up, test, and rework increase the cost of the module. Further,
the multiple steps increase the likelihood of errors during rework and of
damaging the module or the computer by repetitively removing and installing the
module in the two computer systems.

Detailed Description Text - DETX (3):
The **power-up** sequence for IBM AT computers is well known in the art.

Briefly, at power turn-on, the CPU 12 issues a hardware reset to all modules in
the computer 10 to instruct each module to start an initialization routine.
The CPU 12 reads instructions for a basic input/output system (BIOS) from a
programmable read only (PROM) 13 located on the CPU module. After executing a
plurality of initialization routines from the BIOS, the CPU 12 reads utility
programs from the memory. The utility programs are previously stored into one
of the memory devices, preferably the hard disk 16, and identify the modules
that are expected to be connected to the AT bus 14 and execute initialization
and diagnostic routines on the modules and their interfaces to the AT bus.

Detailed Description Text - DETX (41):
On the other hand, if the system does not properly boot up, it is assumed
that there is a conflict in the memory address between the ethernet interface
module 26 and another add-on module in the computer 10 (step 306). If there is
a memory conflict, the CPU 12 halts during the system power up. To resolve the
conflict, the Ethernet interface module 26 is removed from the computer 10
(step 310) and installed in a second computer system (step 312). The second
system is used to determine whether the Ethernet interface module 26 operates
properly by reducing the probability of a memory base address conflict. The
second system has the same basic configuration as the first system but
preferably does not have any add-on modules, thereby precluding a memory
conflict between the Ethernet interface module 26 and an add-on module. In
addition, in the jumperless mode, the second system is used to reprogram the ID
memory 36 with a different memory base address, as will be described below.
After **inserting** the Ethernet interface module 26 into the second system, the
second system is powered up. If the second system boots up properly (step
314), the Ethernet interface module 26 is presumed to be operational and that
the problem in the first system was a memory conflict. Thus, it is

necessary
to reallocate the memory base address location of the Ethernet interface module
26 to eliminate the conflict (step 316).

Detailed Description Text - DETX (45):
If the second system does not properly boot up at step 314, the configuration byte of the memory is reconfigured as described above at step 316
(step 318). The second system is again attempted to be rebooted at step 314.
Alternatively, instead of reconfiguring the memory location at step 318 the
module may be **inserted** into another system (step 320) and the other system
rebooted as described above for step 314.